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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/092,526

03/08/2002

Hisao Shigematsu

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11/12/2004

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EXAMINER

BROCK II, PAUL E

ART UNIT

PAPER NUMBER

2815

DATE MAILED: 11/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/092,526

Applicant(s)

SHIGEMATSU ET AL.

Examiner

Paul E Brock II

Art Unit

2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 August 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 13-24 and 26 is/are pending in the application.
- 4a) Of the above claim(s) 14, 16, 18, 19, 22-24 and 26 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 13, 15, 17, 20 and 21 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 08 March 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☒ Certified copies of the priority documents have been received in Application No. 09/191,543.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>7-9-04</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Election/Restrictions

1. Applicant's election of Species I, claims 13, 15, 17, 20, 21, and 25 in Paper No. 6 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).
2. Claims 14, 16, 18, 19, 22 – 24, and 26 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected species, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 6.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 13, 15, 17, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimawaki (USPAT 5903018) in view of Tanoue et al. (USPAT 5598015, Tanoue).

With regard to claim 13, Shimawaki discloses in figures 3 – 7 a method for fabricating a semiconductor device. Shimawaki discloses in figure 3 forming a first semiconductor layer (4) over a semiconductor substrate (1). Shimawaki teaches in figure 3 and column 5, lines 31 – 32 wherein the semiconductor substrate is made of a GaAs semiconductor substrate. Shimawaki is silent to the substrate being formed of an InP semiconductor substrate. Tanoue teaches in figures 1 – 11 and column 3, lines 30 – 31 wherein a first semiconductor layer (2/3) is formed over an InP substrate. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the InP substrate of Tanoue in the method of Shimawaki in order to increase the cutoff frequency of the device by selecting materials that can be used for the same purpose as stated by Tanoue in column 5, lines 27 – 42, column 5, lines 48 – 49, and column 6, lines 9 – 29. (See MPEP 2144.06 and 2144.07). Shimawaki discloses in figure 3 and column 5, lines 29 – 55 and column 7, lines 54 – 60 forming a base layer (5) of a carbon doped $Ga_xIn_{1-x}As_ySb_{1-y}$ layer on the first semiconductor layer. Shimawaki discloses in figure 3 forming a second semiconductor layer (7) on the base layer. Shimawaki discloses in figure 4 patterning the second semiconductor layer in a mesa shape. Shimawaki discloses in figure 6 and column 6, lines 40 – 55 forming a base contact layer (12) on the base layer exposed by patterning the second semiconductor layer. Shimawaki discloses in figure 6 forming a base electrode 14 on the base contact layer. Shimawaki discloses in figure 7 and column 5, lines 29 – 55 wherein the second semiconductor layer is an emitter layer of an AlGaAs layer. Shimawaki does not teach that the emitter layer is of an InP layer. Tanoue teaches in figures 1 – 11 and column 3, lines 30 – 31 in which a second semiconductor layer is an emitter layer of an InP layer. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the InP

Art Unit: 2815

emitter of Tanoue in the method of Shimawaki in order to increase the cutoff frequency of the device by selecting materials that can be used for the same purpose as stated by Tanoue in column 5, lines 27 – 42, column 5, line 51, and column 6, lines 9 – 29. (See MPEP 2144.06 and 2144.07).

With regard to claim 15, Shimawaki discloses in figure 3 and column 6, lines 5 – 6 wherein in the step of forming the base layer, the base layer of an InGaAs layer which corresponds to the $\text{Ga}_x\text{In}_{1-x}\text{As}_y\text{Sb}_{1-y}$ layer whose As composition y is 1.

With regard to claim 17, Shimawaki discloses in figure 6 and column 6, lines 40 – 55 wherein in the step of forming the base contact layer, the base contact layer is formed of a material which lattice matches with a material forming the base layer. It should be noted that lattice matching results from the MOMBE (metal organic molecular beam epitaxy) process used to form the base contact layer.

With regard to claim 21, Shimawaki discloses in figure 5 after the step of patterning the second semiconductor layer, a step of forming a sidewall insulation film (18) on a sidewall of a mesa of the second semiconductor layer.

5. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shimawaki and Tanoue as applied to claim 13 above, and further in view of Hashimoto et al. (USPAT 5846869, Hashimoto).

Shimawaki discloses in figure 6 and column 6, lines 1 – 13 and 50 – 51 depositing the base layer by MOCVD epitaxial deposition process. Shimawaki and Tanoue are silent to, before the step of forming the base contact layer, a step of thermal treating for eliminating

Art Unit: 2815

hydrogen in the base layer. Hashimoto teaches in figures 18 – 20 and column 11, line 56 – column 12, line 31, before the step of forming a layer overlying a base layer, a step of thermal treating for eliminating hydrogen in the base layer introduced during the deposition of the base layer by an epitaxial process. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the thermal treating of Hashimoto before the step of forming the base contact layer in the method of Shimawaki and Tanoue in order to improve the amplification factor of the bipolar transistor as stated by Hashimoto in column 11, line 56 – column 12, line 31. It would have been further obvious in the method of Shimawaki, Tanoue, and Hashimoto the eliminated hydrogen would have been due to the epitaxial MOCVD process of Shimawaki. It should further be noted that the limitation “for eliminating hydrogen” is an intended use limitation that is met by the combination of Shimawaki, Tanoue, and Hashimoto.

Response to Arguments

6. Applicant's arguments with respect to claims 13, 15, 17, 20, and 21 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (571) 272-1723. The examiner can normally be reached on 8:30 AM - 5:30 PM.

Art Unit: 2815

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul E Brock II

A handwritten signature in black ink, reading "Paul E Brock II" with a stylized flourish at the end.